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| EXAMINER | |
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| JOHNSON, BRIAN P | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/699,571 | DOCKSER, KENNETH | |
| | **Examiner** | **Art Unit** | |
| | BRIAN P. JOHNSON | 2183 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on _14 June 2008_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) _1,4,7-10 and 21-34_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1,4,7-10 and 21-34_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1, 4, 7-10, and 21-34 are pending.

### *Papers Filed*

2. Examiner acknowledges receipt of an appeal brief filed on 14 June 2007.

### *Claim Objections*

1. Objections are withdrawn in light of Applicant's amendments.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4, 7-9, 21-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (U.S. Patent No. 5,187,796) in view of Matsuo (U.S. Patent No. 5,901,301)

4. As per claim 1, Wang discloses a microprocessor, comprising:

a vector unit (Fig. 3 ALUs 46, 48 and 50) to execute a vector instruction to perform a first operation on a first set of data operands and a second operation on a

second set of operands. *The examiner asserts that the processor performs a multiply followed by an operand rotate right for the FMULR instruction listed in the col. 27 table. Both operations (multiply and rotate) operate on both sets of operands.*

Wherein the vector instruction includes a first register field indicative of a first primary register in the primary register file and a first secondary register in the secondary register file, a second register field indicative of a second primary register in the primary register file and a second secondary register in the secondary register file, and a third register field indicative of a third primary register in the primary register file and a third secondary register in the secondary register file; and

Wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (Fig. 3 register files 40 and 42, col 27 lines 22-24 and col 27 table). *The examiner asserts that complex pairs of real and imaginary numbers are simply alternate labels for two-dimensional vector data. The data stored in register file 40 corresponds to an "x" vector, and constitutes a real portion of a number and the data stored in register file 42 corresponds to a "y" vector and constitutes an imaginary number. This is considered to be the "primary" and "secondary" register file as claimed. See col 8 lines 47-53.*

Wang fails to disclose 3-input execution units.

Matsuo discloses wherein a 3-input primary floating point unit is configured to multiply first and third operands and further configured to add the second operand to or subtract the second operand from the resulting product. (Col. 27 lines 47-52)

Matsuo discloses his invention to promote "high-speed digital signal processing" by taking advantage of "processing frequently used in signal processing such as a multiply-add operation at high speeds." (Matsuo col. 1 lines 13-16) Wang discloses "DSPs were developed to exploit the successive multiply/accumulate nature of signal processing." (Wang col. 3 lines 24-26) Matsuo's desired outcome of higher processing speeds through optimizing common instructions coincides with that of Wang.

It would have been obvious to one of ordinary skill in the art at the time of invention to have included Matsuo's method of adding a third operand to the product of first and second operands in Wang's invention for the benefit of higher speed processing. The combination would logically require that each of the i, j, and k portions to have separate execution units (as shown in Wang fig 4) that include three inputs that complete a separate multiply-accumulate for each dimension.

5. As per claim 4, Wang/Matsuo discloses the microprocessor of claim 3, wherein the vector unit includes a primary floating point unit (Fig. 3 FPU 46) and a secondary floating point unit (Fig. 3 FPU 48), wherein the primary floating point unit is configured to perform a floating point operation on the first set of operands and the secondary floating point unit is configured to perform a floating point operation on the second set of operands. The addition of Matsuo discloses 3-input execution units. *Col. 27 table lists*

*instructions as "floating point operations", hence, the FPUs are configured to perform floating point operations.*

6. As per claim 7, Wang discloses the microprocessor of claim 2, wherein the vector unit is further characterized as being enabled to perform a cross instruction in which the first and second operations both use at least one operand from the primary register file and at least one operand from the secondary register file. (Col. 26 lines 22-45)

7. As per claim 8, Wang discloses the microprocessor of claim 2, wherein the vector unit is further characterized as being enabled to perform a cross-replicate vector instruction in which the first and second operations are both performed using at least one common operand. *The examiner asserts that the FMULR operation performs a multiply, and then a component rotate using the same operands as the multiply.*

8. As per claim 9, Wang discloses the microprocessor of claim 2, wherein the vector unit is configured to store a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file. *The examiner asserts that complex pairs of real and imaginary numbers are simply alternate labels for two-dimensional vector data. The data stored in register file 40 corresponds to an "x" vector, and constitutes a real portion of a number and the data stored in register file 42 corresponds to a "y" vector and constitutes an imaginary number.*

1. Regarding claim 21, Wang discloses the microprocessor of claim 1, wherein the second set of operands include a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (col 8 lines 53-59).

2. Regarding claim 22, Wang/Matsuo discloses the microprocessor of claim 4 wherein the first operation includes multiplying two of the three first set of operands to obtain a first product and adding or subtracting the remaining of the first set of operands to or from the first product and wherein the second operation includes multiplying two of the three second set of operands to obtain a second product and adding or subtracting the remaining of the second set of operands to or from the second product (Matsuo (col 27 lines 47-52)

3. Regarding claim 23, Wang discloses the microprocessor of claim 22, wherein the first and second sets of operands comprise first and second set of floating point formatted operands (col 27 table—note “floating-point operations”).

4. Regarding claim 24, Wang discloses the microprocessor of claim 1, wherein the vector register file wherein the vector instruction includes a target register field indicative of a primary target register in the primary register file and a secondary target register in the secondary register file (fig. 14 and col 24 lines 49-51) and further

wherein the vector unit is further configured to store a result of the first operation in the primary target register and to store a result of the second operation in the secondary target register. *Examiner asserts that vector registers 40 and 42 can store the result of the first and second operands.*

5. Regarding claim 25, Wang/Matsuo discloses a vector trait to process a vector instruction having an opcode and first, second, and third register fields (col 27 table), comprising: a register file including a primary register file having a set of primary registers (fig 3 reference 40) and a secondary register file having a set of secondary registers (fig. 3 reference 42), wherein the register field identifies a register in the primary register file and a corresponding register in the secondary register file (col 8 lines 48-53— “i” and “j” portions); primary and secondary calculating units (fig. 4 reference 46 and 48), wherein the primary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands and wherein the secondary calculating unit includes fast, second, and third inputs to receive, respectively, first, second, and third operands of a second set of operands (Matsuo Col. 27 lines 47-52) and multiplexing circuitry controlled by the opcode to select each of the first, second, and third operands in the first and second set of operands from the set of primary and secondary file registers identified by the register fields. *Examiner asserts that multiplexing circuitry inherently exists because different inputs are required to enter the execution units for different calculations.*

6. Regarding claim 26, Wang/Matsuo discloses the vector unit of claim 25, wherein the multiplexing circuitry is controlled by the opcode to select: the first operand in the first set of operands from either the first primary or the first secondary registers (col 27 table—*Examiner asserts that the opcode controls the register value that enters the execution unit; therefore, it control the multiplexing circuitry*); the second operand in the first set of operands from either the second primary or the second secondary registers (col 8 lines 53-59); and the third operand in the first set of operands from either the third primary or the third secondary registers (col 8 lines 53-59); the first operand in the second set of operands from either the first primary or the first secondary registers, the second operand in the second set of operands from either the second primary or the second secondary registers; and the third operand in the second set of operands from either the third primary or the third secondary registers (col 8 lines 53-59 and col 27 table).

**7.** Regarding claim 27, Wang/Matsuo discloses the vector unit of claim 25, wherein the primary calculating unit is controlled by the opcode to perform a first operation on the first set of operands and the secondary calculating unit is controlled by the opcode to perform a second operation on the second set of operands (Matsuo Col. 27 lines 47-52—*Examiner asserts that the MAC opcode would control the execution units of both primary and secondary portions*).

8. Regarding claim 28, Wang/Matsuo discloses the vector unit of claim 27, wherein the first operation differs from the second operation.

*Examiner asserts that the operations are completed on two different sets of operands, therefore, the two operations differ.*

9. Regarding claim 29, Wang/Matsuo discloses the vector unit of claim 27, wherein the first and second operations both include multiplying their respective first and third operands to obtain respective first products and adding or subtracting their respective second operands to or from the respective first products (Matsuo Col. 27 lines 47-52).

10. Regarding claim 30, Wang/Matsuo discloses the vector unit of claim 25, wherein the first, second, and third operands of the first and second sets of operands are all floating point formatted operands (col 27 table).

11. Regarding claim 31, Wang/Matsuo discloses a microprocessor including: an execution unit enabled to execute an asymmetric instruction, wherein the asymmetric instruction includes a set of three operand register fields and a target register field and an operation code (opcode) (col 24 lines 49-51); a register file accessible by the execution unit and having a rank of two including a primary register file (fig 3 reference 40) and a secondary register file (fig 3 reference 42) wherein a value in an operand register field identifies a register in the primary register file and

a corresponding register in the secondary register file (col 8 lines 53-59); wherein the execution unit is configured to perform a first operation on a first set of three operands (Matsuo Col. 27 lines 47-52) selected from registers identified by the set of operand register fields and to perform a second operation on a second set of three operands also selected from the registers identified by the set of operand registers fields (see combination) wherein the first and second operations and. selection of the first and second sets of operands are determined by the opcode.

Examiner asserts that the opcode determines that the operands are of type multiply-accumulate.

12. Regarding claim 32, Wang/Matsuo discloses the microprocessor of claim 31, where at least one condition selected from the group of conditions consisting of the first and second operations being different and the first and second sets of operands being different is true.

*Examiner asserts that the operands are different (i.e. one includes the “i” operands and the other includes “j” operands). Consequently, the operations are considered to be different.*

13. Regarding claim 33, Wang/Matsuo discloses the microprocessor of claim 31, wherein the execution unit is further configured to store a result of the first operation in a register of the primary register file determined by the target register field and

the result of the second operation in a register of the secondary register field also determined by the target register field (Matsuo Col. 27 lines 47-52).

14. Regarding claim 34, Wang/Matsuo discloses he microprocessor of claim 31, including multiplexing circuitry controlled by the opcode to select a first of the first set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the first set of three operands from a second primary and a second secondary register identified by a second operand register field, a third of the first set of three operands from a third primary and a third secondary register identified by a first operand register field (col 8 lines 53-59) , a first of the second set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the second set of three operands from a second primary and a second secondary register identified by a second operand register field, and a third of the second set of three operands from a third primary and a third secondary register identified by a first operand register field (col 27 table).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang/Matuo in view of Golliver et al. (U.S. Publication No. US 2002/0004809) hereinafter referred to as Golliver.

10. As per claim 10, Wang/Matuo discloses the microprocessor of claim 9, but fails to disclose wherein the vector unit is configured to perform a complex operation in which

the imaginary portion of a first operand is multiplied by an imaginary portion of a second operand in the first operation and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation.

11. Golliver discloses a vector unit configured to perform a complex operation in which the imaginary portion of a first operand is multiplied by an imaginary portion of a second operand in the first operation (AiBi in Fig. 3A) and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation (AiBr in Fig. 3A).

12. Golliver discloses “a data manipulation instruction for enhancing value and efficiency of performing complex arithmetic instructions.” (Paragraph 2) Golliver’s desired outcome coincides with that of Wang: increased efficiency of processing.

13. It would have been obvious to one of ordinary skill in the art at the time of invention to have included Gollivers method of complex number arithmetic in Wang’s processor for the benefit of increased processing efficiency.

### *Response to Arguments*

15. Applicant's arguments filed in the appeal brief have been fully considered but they are not all persuasive.

### Argument 1: Claims 1, 7-9, 21, 23 and 24

*Wang does not anticipate Appellant's Claim 1 because Wang does not describe a vector execution unit for instructions having three operand registers in which all of the operands are provided by a rank-of-two register file (i.e., a register file have a primary register file and a secondary register file), where the selection of the operands occurs from one of six (2x3 registers per file) total register fields within the two*

*register files. Rather, Wang provides a vector unit having three separate register files (reference numerals 40, 42, and 44), which each receive a single input.*

*Also, Wang's illustrated table at col. 27, lines 22-24 provides an instruction naming scheme that enables three-dimensional vector processing. However, that table does not teach the vector instruction having the characteristics and associated functionality of the three register fields within the instruction being respectively indicative of a first/second/third register in the first register file or a first/second/third register in the second register file.*

**Examiner's Response**

The following is Examiner's understanding of Applicant's arguments, broken down and addressed.

**Argument A: Wang does not disclose the rank-of-two register file.**

It is presumed that the "rank-of-two" limitation to which Applicant refers is regarding the "primary" and "secondary" labels of the register files in Applicant's claims. It is noted that these labels have no definition associated with them that would give them patentable weight.

In the current interpretation, Wang discloses two register files (Fig. 3 references 40 and 42) which store registers for the X-dimension and Y-dimension, respectively. The X register file (Fig. 3 reference 40) is interpreted to be the primary register file of Applicant's claims. The Y register file (Fig. 3 reference 42) is interpreted to be the secondary register file. There are no limitations within the claim that make this interpretation unreasonable.

**Argument B: Applicant alleges that Wang discloses three separate register files, rather than the two as claimed.**

Examiner notes that the third register file used for the Z-dimension does not prevent the claims from being properly rejected. Applicant's claim 1 uses the language "comprising" rather than "consisting". This means that additional circuitry (including an additional register file) does not disqualify Wang as properly applied prior art.

**Argument C: The table in col. 27 of Wang does not show three register fields indicative of a first/second/third register in the first register file or a first/second/third register in the second register file.**

Applicant is partially correct. To clarify, each of the register files 40, 42, and 44 have 64 registers. Note col 8 lines 48-64. This is interpreted to be 64 register fields. Three of these 64 register fields are used to rejection the three fields mentioned in the claim language.

Also note col 9 lines 9-28. It discloses that the three execution units 46, 48 and 50 are associated to the X, Y, and Z dimension respectively. This means, of course, that the register files 40, 42, and 42 exclusively respectively provide inputs for execution units 46, 48 and 50. It is also clear from the citations that each of these execution units contains two inputs. This is where the rejection becomes improper.

Applicant's claims require that a single instruction contain 3 operands, each from one of the three fields of the primary or secondary register file. However, Wang discloses only two inputs to these register files.

An obvious-type rejection has been made to remedy this deficiency. In particular, Matsuo has been added to the rejection of Claim 1. As combined,

Wang/Matsuo contains three operand inputs for a vector register unit (either 46 or 48) that takes inputs from each of the register fields (here, three of the 64 possible registers) from the primary or secondary register file.

Furthermore, Examiner concedes that execution unit 46 (for example) only accepts inputs from the X-dimension (or “primary register file”); however, it is noted that the claim requires that the vector execution unit take operands from the first three register fields of the primary register file <u>OR</u> the secondary register file. Here, of course, units 46 and 48 take operands from X or Y dimension exclusively. So, the rejection is still proper.

**Argument 2: Claims 4, 10 and 22**

*Wang is devoid of any teaching (or suggestion) of a pair of 3-input (execution) units. Specifically, Wang is devoid of any teaching of (a) two sets of three operands that feed into (b) two respective 3-input units (3-input primary and 3-input secondary units). Further, Wang's described system does not have a three input execution unit configuration in which the three inputs are retrieved from first, second or third register fields within two register files.*

**Examiner’s Response**

This issue is addressed above. It is true that Wang alone does not have three inputs to the execution unit. An obvious type rejection is made for this reason.

**Argument 3: Claims 4, 10 and 22 (cntd)**

*Matsuo also fails to teach or suggest the pair of three input arithmetic units, which receive three operands from two register files. Matsuo at col. 27, lines 47 - 52 provides a "3- operand instruction," which is "'[a] 'mac' instruction for multiply-add operation." This 3- operand instruction is the instruction received by the processing unit for execution and completes the multiplication of two register values (Rsrcl and Rsrc2) followed by addition of "the value in the pair of registers specified by Rdest" to the result of the multiplication. Notably, the functional description of the execution of the 3-operand instruction makes clear that the 3- operand instruction of Matsuo does not simultaneously provide three operands to a single 3-input arithmetic unit or, for that matter, to two such 3-input arithmetic units. Rather, only two operands are provided to the (second) operating unit at a time.*

**Examiner's Response**

Applicant argues that the multiply-accumulate function does not provide three operands to the execution unit "at a time" or "simultaneously." Examiner does not concede this put, but respectfully notes that this limitation is in no way required by the claim. Claim 4, states the following:

*4. (previously presented) The microprocessor of claim 1, wherein the vector unit includes a 3-input primary unit and a 3-input secondary unit, wherein the primary unit is configured to perform the first operation on the first set of operands and the 3-input secondary unit is configured to perform the second operation on the second set of operands.*

There is no timing requirement ever mentioned. It is only required that an operation is completed on a "first set of operands." In this case, the operation is a multiply-accumulate operation found in Matsuo. Examiner further notes that the Wang/Matsuo combination is viewed when the multiply-accumulate instruction is applied twice. In that case, the primary unit (execution unit 46) completes an operation (multiply-accumulate) on three operands (Rsrc1, Rsrc2, and Rdest) from three register fields (of the 64 available in register file 40) as required by the claim. Then, a subsequent operation (another multiply accumulate) is completed on the secondary unit (execution unit 48) on three operands (the second set of Rsrc1, Rsrc2, and Rdest) from three separate register fields (of the 64 available in register file 42). The claim limitations have been entirely met.

Examiner further notes that a destination can be an operand as well. In fact, this is the case for the multiply accumulate. Rdest is very clearly an operand in the operation.

**Argument 4: Claims 25 and 31 (and 26-30, 32-24)**

*The rejections of Claims 25 and 31 should also be reversed for the same reasons provided above. Claim 25 recites: "primary and secondary calculating units, wherein the primary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands and wherein the secondary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a second set of operands; and multiplexing circuitry controlled by the opcode to select each of the first, second, and third operands ... from the set of primary and secondary file registers..." (emphasis added). Claim 31 recites: "asymmetric instruction includes a set of three operand register fields ... wherein the execution unit is configured to perform a first operation on a first set of three operands selected from registers identified ... and to perform a second operation on a second set of three operands also selected from the registers..." (emphasis added).*

**Examiner's Response**

These limitations are addressed above.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Seshan (U.S. Patent No. 6,061,787) discloses a processor consisting of multiple parallel register files.

Tromp et al. (U.S. Publication No. US 2005/0283592) disclose a system executing two operations based on a single instruction.

Gochman et al. (U.S. Patent No. 6,920,546) disclose a system with multiple operations in an instruction word sharing common operands.

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made.

The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183